REMARKS

The above amendments and these remarks are submitted in reply to the Office Action dated August 10, 2004.

I. Summary of the Examiner's Objections/Rejections

The specification has been objected to for containing several typographical errors. The drawings have been objected to for including a reference numeral not mentioned in the description. Claims 1-2 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Kau, et al. (U.S. Patent No. 5,684,997), Favor, et al. (U.S. Patent No. 6,093,213) and "knowledge commonly known in the art" as provided by Microsoft Press Computer Dictionary, 3rd Edition (Microsoft). Claims 2-6 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Kau, et al. and Favor, et al. Claim 2 stands objected to for containing an informality. Claim 6 stands objected to for containing an informality.

II. Summary of the Applicant's Amendments

The specification has been amended to correct minor typographical and grammatical errors present therein, and to make the description correspond to the originally filed drawings. Claims 2-3 and 5-6 have been amended. The Applicant asserts that no new matter has been added by such amendments.

III. Objection to the Specification and Drawings

By this Amendment, the specification has been amended to correct minor typographical and grammatical errors present therein, including the typographical errors noted in paragraph 13 of the instant Office Action. Additionally, the specification has been amended such that the description corresponds to the originally filed drawings. The Applicant submits that no new matter has been added by such amendments. Accordingly, reconsideration of the objection to the specification and drawings is respectfully requested.

IV. Objection to Claims 2 and 6

By this Amendment, Claim 2 has been amended to include the proper phrase "I/O" as noted by the Examiner in paragraph 10. Accordingly, reconsideration of the objection to Claim 2 is respectfully requested.

By this Amendment, Claim 6 has been amended to be dependent upon Claim 5. Accordingly, reconsideration of the objection to Claim 6 is respectfully requested.

V. Rejection of Claims 1-2

The Applicant traverses the rejection of the aforementioned claims for the reasons set forth in greater detail below. On page three of the instant Office Action, in rejecting Claim 1, the Examiner combines the teachings of Kau, et al. and Favor, et al. in combination with taking Official Notice "...of a timer for measuring time intervals..." as being well known in the art and citing the aforementioned Microsoft Dictionary for the definition thereof. However, the Applicant would like to point out that neither the Kau, et al. nor Favor et al. references require the use of a timer. The only teaching or suggestion of using a timer "...that is triggered by reads of zero from the update-in-progress status bit..." is found in the Applicant's disclosure- which cannot form the basis of an obvious rejection. MPEP 2143. Accordingly, the aforementioned combination of references as cited by the Examiner is improper and should be withdrawn.

Notwithstanding the inappropriateness of combining the aforementioned references, the Applicant's submit that the combined references also do not render the claimed invention obvious. The instant invention is directed to a system, software and method for improving SMI latency in a system. As defined in Claim 1, an exemplary system includes the following limitations which are not taught or suggested in the references either individually or in combination:

> "...a status latch for storing the status of the timer, which status is read using a status bit;" and
>
> "...SMI handling code that reads the status latch, and if the status latch is zero, exits the SMI handling code, and if the status latch is non-zero, writes to a second register location, reads a third register location, and if a predetermined bit of the value read from the third register location is set, repeats the previous two steps until the value of the bit is not set, and then exits the SMI handling code..."

As the aforementioned combination of limitations are not taught or suggested in the combination of references as cited by the Examiner, the invention as defined in Claim 1 is not rendered obvious over Kau, et al. and Favor, et al. in addition to the Official Notice taken by the Examiner.

As understood, Kau, et al. as disclosed, for example, at col. 129, line 54 – col. 130, line 21 is directed to a computer system that employs conventional interrupt handling functionality. As specifically described, for example, at col. 130, lines 10-13 "...End of Interrupt (EOI) causes an ISR bit to be reset. A specific CPU EOI command, or the priority resolver clearing the highest-priority ISR bit (nonspecific EOI), can determine which ISR bit should be reset..." Thus, as is conventionally done, when an interrupt is finished being serviced, the ISR which indicates that an interrupt is being handled is reset once the interrupt is completed and subsequent interrupts are serviced. This reference does not appear to discuss how to reduce SMI latency within a system, as the interrupt is executed to completion before another interrupt is processed, nor does it describe a system having the structure as defined in Claim 1. The Examiner even admits this shortcoming on page three of the instant Office Action, by stating that "...Kau, et al. does not teach a status latch for storing the status of the timer, which status is read using a status bit..."

To overcome the aforementioned shortcomings, the Examiner takes Official Notice of the use of registers and provides a definition thereof as provided in the Microsoft Dictionary. However, this reference also does not provide a definition of a status latch or how the same is used to reduce SMI latency within a system as defined in Claim 1. Further, the Examiner combines the teachings of Favor, et al. with the combined teachings of Kau, et al and the Microsoft reference to overcome the aforementioned shortcomings. However, such combination still does not render the claimed invention obvious as Favor, et al. does not teach or suggest the aforementioned limitations that the Examiner admits are not present in Kau, et al.

More specifically, in rejecting Claim 1, the Examiner equates the control register of Favor, et al. as being "...equivalent to both a latch and a status latch, which is set if an SMI is not running when another SMI is asserted and cleared when the another SMI is deasserted..." However, such equivalence is not proper as the control register of Favor,

et al. does not function as both the latch and the status latch as submitted by the Examiner as such components perform different operations. As described, for example, col. 34, lines 59-62 of Favor, et al. "A SMM mask 970 furnishes interrupt masking while the processor 120 is in SMM, as indicated by an asserted SMM control register bit 988..." Thus, as understood, the control register provides a signal that effectively masks interrupts while the larger system is in SMM. Such functionality is different from "...a status latch for storing the status of the timer, which status is read using a status bit..." as the masking operation of the control register does not appear to be dependent, for example, upon "the status of the timer"; the control register is only used to provide a masking signal In like manner, the masking signal provided by the control register also is submitted as not being equivalent to "...a latch that is set if the timer is running when a system management interrupt is asserted and cleared when SMI is deasserted..." as the disclosure does not indicate or provide such details. In any event, the functions performed by the latch and status latch of Claim 1 are not equivalent, but dependent upon one another, and therefore, cannot be equivalent to a single component as asserted by the Examiner. Therefore, the single (e.g. control register) component of Favor, et al. is not equivalent, and therefore, does not teach or suggest both of the latch and status latch as recited in Claim 1. Thus, Favor, et al. does not render the invention as defined in Claim 1 or the components submitted by the Examiner obvious. Consequently, the combination of Kau, et al. Favor, et al. and the Microsoft does not render the invention as defined in Claim 1 obvious. Accordingly, reconsideration of the rejection of Claims 1 is respectfully requested.

Claim 2 depends upon and includes the limitations of Claim 1 and is allowable for at least the reasons set forth above with respect to Claim 1. Accordingly, reconsideration of the rejection of Claims 1-2 is respectfully requested.

VI. Rejection of Claims 3-6

The Applicant traverses the rejection of the aforementioned claims for the reasons set forth in greater detail below. Claim 3 is directed to a method for improving SMI latency of a system, including the limitations of "...reading the status latch..." and

"...stopping if the value read from the status latch is zero..." which are not taught or suggested in the combination of references as cited by the Examiner. As discussed in greater detail above, Kau, et al. discloses conventional interrupt handling where an "...[e]nd of Interrupt (EOI) causes an ISR bit to be reset. A specific CPU EOI command, or the priority resolver clearing the highest-priority ISR bit (nonspecific EOI), can determine which ISR bit should be reset..." However, as admitted by the Examiner on page five, paragraph 5 of the instant Office Action, "...Kau does not teach a status latch; reading the status latch; and stopping if the status latch is zero..." To overcome the aforementioned shortcoming, the Examiner added the teachings of Favor, et al. and states that "...Favor teaches a status latch...and stopping when a read of the status latch returns a result of zero (See Column 34, lines 46-67)..." However, that portion of Favor, et al. does not teach or suggest what the Examiner is asserting. More specifically, the only part of the cited section that deals with the control register (which the Examiner is equating with the status latch) is found at col. 34, lines 59-62, which state in relevant part:

> "...A SMM mask 970 furnishes interrupt masking while the processor 120 is in SMM, as indicated by an asserted SMM control register bit 988. Specifically, SMM mask 970 masks recognition of pending NMI, ResetCPU and SMI interrupts..."

Nowhere within the specific portion of Favor, et al. cited above, nor in the larger portion as cited by the Examiner is there a teaching or suggestion of "...stopping, if the value read from the status latch is zero..." Consequently, the combination of Kau, et al. and Favor, et al. does not render the invention as defined in Claim 3 obvious. Accordingly, reconsideration of the rejection of Claim 3 is respectfully requested.

Claim 4 depends upon and includes the limitations of Claim 3 and is submitted to be allowable for at least the reasons set forth above with respect to Claim 3. Accordingly, reconsideration of the rejection of Claims 3-4 is respectfully requested.

Claim 5 is directed to software for improving SMI latency within a system. Claim 5, like Claim 3 above, includes limitations directed to "...reads the status latch..." and "...exits if the value read from the status latch is zero..." As such, Claim 5 is submitted to be allowable at least for the reasons set forth above with respect to Claim 3. Accordingly, reconsideration of the rejection of Claim 5 is respectfully requested.

Claim 6 depends upon and includes all the limitations of Claim 5 and is submitted to be allowable at least for the reasons set forth above with respect to Claim 5. Accordingly, reconsideration of the rejection of Claims 5-6 is respectfully requested.

CONCLUSION

In view of the above amendments and remarks, it is respectfully submitted that Claims 1-6 are now in proper condition for allowance and such action is earnestly solicited.

The Commissioner is hereby authorized to charge any underpayments or credit any over payments to Deposit Account No. 16-1520 for any payment in connection with this communication, including any fees for extension of time, which may be required. The Examiner is invited to call the undersigned if such action might expedite the prosecution of this application.

Respectfully submitted,
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Date: 2/10/05

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